

3 memory module including a memory module controller, the method comprising [the  
4 steps of]:

5 sending a first memory transaction from the system memory controller to the  
6 memory module controller, the first memory transaction having a first format;  
7 reformatting the first memory transaction into a second memory transaction  
8 for [the] at least one of the memory devices, the second memory transaction  
9 having a second format that is different from the first format; and  
10 sending the [reformatted] second memory transaction to the at least one of  
11 the memory devices.

1 19. (Unchanged) The method of claim 18, wherein the memory transaction is a  
2 read transaction.

1 20. (Unchanged) The method of claim 18, wherein the memory transaction is a  
2 write transaction.

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#### REMARKS

Reconsideration of this application, as amended, is respectfully  
requested. The following remarks are responsive to the Office Action mailed on  
September 3, 1999.

The specification is objected to for minor informalities. The title of the  
invention is objected as being non-descriptive.

Claims 1-6, 9, 13, and 15-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Memory Systems Design and Applications, edited by Dave Bursky, pp. 213-220 ("Bursky").

Claims 7, 8, 10-12, and 14 stand rejected under 35 U.S.C. §103(a) as unpatentable over Bursky.

Claims 1-20 stand provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of co-pending Application No. 09/023,172 and claims 1-17 of co-pending Application No. 09/023,234.

Claims 1-20 are pending. Claims 1-10 and 15-18 have been amended. Applicant respectfully submits that no new matter has been introduced by the amendments made herein.

The Examiner has objected to the specification on page 2 for missing serial numbers. Accordingly, the specification has been amended to provide the appropriate serial numbers.

The Examiner has objected to the title of the invention as being non-descriptive. Accordingly, the title of the invention has been amended. Applicant respectfully submits that the amended title is clearly indicative of the invention to which the claims are directed.

Claims 1-6, 9, 13, and 15-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Bursky. In particular, the Examiner states:

Regarding claims 1, 17, and 18 on page 217 Bursky teaches in the photo caption that "System costs plummet when function duplication is designed out. While most minis duplicate read/write

and control electronics for each board of memory DIPs, Interdata makes one read/write/control set serve more memory, by using eight little 'daughter boards.' The packaging also simplifies reconfiguration and speeds up field repair" (emphasis added).

Furthermore, on page 219, third column, he writes that "The PC-board economy is possible through the use of 'daughter boards,' strips that are 8 in. long, 1 in. wide and plug into the 15x15 in. memory board itself. Not only does this mean that 256 k-bytes can be packed on the board instead of 32 or 64 k-bytes, it also means that function duplication is cut back. As a result, the read/write control logic that would have been duplicated on a series of 64 k-byte boards appears just once on the 15x15 in. motherboard, serving all 256 k-bytes. Larry MacPherson, Interdata product manager for the Series Sixteen, points out that this unusual modularity makes it easy to add and subtract memory in the field, and slashes the cost of incremental memory increases" (emphasis added).

Bursky's focus in the passages above is toward the daughter card system of Interdata. However, the underlined passage above teach that it was known to use memory controllers on individual memory modules, each of which contained a plurality of memory device as claimed. In fact, such a design appears to have been the norm. The passages above describe a new (for the time) method of reducing the duplication of the memory controllers by removing them from the memory modules and using a single controller on the motherboard for all memory modules (daughter cards). This is the standard today, and is the admitted prior art of the instant application. However, in 1980 and before, it was common to include the memory controller on each memory module as taught above.

Bursky does not explicitly teach that the motherboard containing the memory modules in which each had their own memory controller like the claimed system memory controller, however it would have been obvious to one skilled in the art at the time of the invention that such a motherboard necessarily included the claimed system memory controller for the proper functioning of the memory module controllers. This broadly claimed system memory controller could be interpreted either as the memory controller presiding over the module memory controllers or as the central processing unit.

Bursky also does not explicitly teach that the memory controller reformats the transactions it receives before passing them on to the plurality of memory devices, however it would have been obvious that such reformatting takes place since memory devices required different format signals than memory controllers.

(Office Action, 2/9/99, p. 3-5).

Applicant respectfully submits that claim 1, as amended, is not anticipated by Bursky. Claim 1 includes the limitations of:

A system comprising:  
a system memory controller; and  
a first memory module comprising:  
a first plurality of memory devices;  
a first memory module controller coupled to the system memory controller and the first plurality of memory devices, the first memory module controller being configured to receive from the system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format, the second format of the second memory transaction being different from the first format of the first memory transaction.

(Claim 1)(emphasis added)

In contrast to claim 1, Bursky fails to disclose or suggest a system having a system memory controller and a first memory module including a first plurality of memory devices and a first memory module controller coupled to the system memory controller and the first plurality of memory devices.

In further contrast to claim 1, Bursky fails to disclose or suggest the first memory module controller being configured to receive from the system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format.

In still further contrast to claim 1, Bursky fails to disclose or suggest the second format of the second memory transaction is different from the first format of the first memory transaction.

Bursky relates generally to providing reliability to memory devices by using error correction capability. See Bursky pp. 216-220. The Examiner, however, relies on the following sections of Bursky to support the §102(b) rejection.

System costs plummet when function duplication is designed out. While most minis duplicate read/write and control electronics for each board of memory DIPS, Interdata makes one read/write/control set serve more memory, by using eight little "daughter boards." This packaging also simplifies reconfiguration and speeds up field repair.

(Bursky p.217, photo caption text).

The PC-board economy is possible through the use of "daughter boards," strips that are 9-in.long, 1-in. wide and plug into the 15x15-in. memory board itself. Not only does this mean that 256 kbytes can be packed on the board instead of 32 or 64 kbytes, it also means that function duplication is cut back.

As a result, the read/write control logic that would have been duplicated on a series of 64-kbyte boards appears just once on the 15x15-in. motherboard, serving all 256 kbytes.

(Bursky p.219).

The Examiner asserts that the above sections of Bursky teach that it was known to use memory controllers on individual memory modules. Applicant respectfully submits that the Examiner's reliance on the above sections of Bursky is misplaced. First, applicant respectfully submits that the above sections of Bursky teach away from the claimed invention by teaching one read/write control logic for a plurality of memory modules. By way of contrast, claim 1 recites a first memory module having a first plurality of memory devices and a first memory module controller coupled to a system memory controller and the first plurality of memory devices.

Second, applicant respectfully submits that the above sections of Bursky do not teach or suggest converting a first memory transaction in a first format into a second memory transaction in a second format by a first memory module controller for a first plurality of memory devices. The Examiner asserts that the read/write/control logic of Bursky teach inherently reformatting of transactions. It is respectfully submitted that this assertion is unsupported. The read/write/control logic taught by Bursky is used to perform read and write transactions for memory devices. Furthermore, nowhere in Bursky does it teach converting a memory transaction in one format into another format.

For the above reasons, applicant respectfully submits that claim 1 is not anticipated by Bursky, and is in condition of allowance. Given that claims 2-16 depend directly or indirectly on claim 1, applicant respectfully submits that claims 2-16 are not anticipated by Bursky, and are in condition of allowance for the same reasons as claim 1.

Applicant respectfully submits that claim 17, as amended, is not anticipated by Bursky. Claim 17 includes the limitations of:

A system comprising:  
a system memory controller;  
a memory bus coupled to the system memory controller; and  
a memory unit including:  
a plurality of memory devices;  
a memory module controller coupled to the memory bus and the plurality of memory devices, the memory module controller being configured to receive a first memory transaction from the memory bus in a first format and to convert the first memory transaction into a second memory transaction in a second format to at least one of the plurality of memory devices, the second format of the second

memory transaction being different from the first format of the first memory transaction.

(Claim 17)(emphasis added).

In contrast to claim 17, Bursky fails to disclose or suggest a system having a memory module controller coupled to the memory bus and the plurality of memory devices. In further contrast to claim 17, Bursky fails to disclose or suggest the memory module controller being configured to receive a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format. In still further contrast to claim 17, Bursky fails to disclose or suggest the second format of the second memory transaction being different from the first format of the first memory transaction.

As mentioned previously, Bursky provides no teaching of converting a memory transaction in one format into another. For the above reasons, applicant respectfully submits claim 17 is not anticipated by Bursky, and is in condition of allowance.

Applicant respectfully submits that claim 18, as amended, in not anticipated by Bursky. Claim 18 includes the limitations of:

A method of communicating a memory transaction between a system memory controller and at least one of a plurality of memory devices on a memory module including a memory module controller, the method comprising:

    sending a first memory transaction from the system memory controller to the memory module controller, the first memory transaction having a first format;

reformatting the first memory transaction into a second memory transaction for the at least one of the

memory devices, the second memory transaction having a second format that is different from the first format; and sending the second memory transaction to the at least one of the memory devices.

(Claim 18)(emphasis added).

In contrast to claim 18, Bursky fails to disclose or suggest a method, which reformats a first memory transaction having a first format into a second memory transaction having a second format that is different than the first format to at least one of the memory devices.

As stated previously, Bursky provides no teaching of converting a memory transaction in one format into another. For the above reasons, applicant respectfully submit that claim 18 is not anticipated by Bursky, and is in condition of allowance. Given that claims 19 and 20 depend on claim 18, applicant respectfully submits that claims 19 and 20 are not anticipated by Bursky, and are in condition of allowance for the same reasons as claim 18.

The Examiner has rejected claims 7, 8, 10-12, and 14 under 35 U.S.C. §103(a) as unpatentable over Bursky. Given that claims 7, 8, 10-12, and 14 depend directly or indirectly on claim 1, applicant respectfully submits claims 7, 8, 10-12, and 14 are not rendered obvious over Bursky for the same reasons claim 1 is not anticipated by Bursky.

The Examiner has provisionally rejected claims 1-20 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-14 of co-pending Application No. 09/023,172 and claims 1-17 of co-pending Application No. 09/023,234.

Upon a condition of allowance of one or more claims, applicant will submit a terminal disclaimer for this application.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the rejections and objections set forth in the Office Action mailed September 3, 1999 have been overcome. Accordingly, applicant respectfully request that claims 1-20, as amended, be found in a condition of allowance.

If a telephone interview will expedite the prosecution of this application, the Examiner is invited to contact Mike Kim at (408) 720-8300 X345.

If there are any additional charges, please charge them to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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